[0022] The semiconductor device according to this embodiment is a vertical device having a current path formed in a vertical direction to connect a first main electrode **1** and a second main electrode **10** provided on top and bottom surfaces of a semiconductor layer, respectively. The semiconductor device according to this embodiment includes a cell section in which the current path is formed, and a terminal section formed on an exterior of the cell section so as to surround the cell section. FIG. **1** illustrates part of the cell section. Other drawings from FIG. **2** on down also show part of the cell section.

[0023] A drain layer (or a substrate) **2** is provided as a first semiconductor layer made of n^+-type silicon having a high impurity concentration. An n-type pillar layer **3**, which is a second semiconductor layer made of n-type silicon, and a p-type pillar layer **4**, which is a third semiconductor layer made of p-type silicon, are provided on a major surface of the drain layer **2**.

[0024] The n-type pillar layer **3** and the p-type pillar layer **4** are arranged alternately adjacent (as a p-n junction) and periodically along a lateral direction generally parallel to the major surface of the drain layer **1**, forming a so-called "super junction structure."

[0025] The planar pattern of the periodical arrangement structure (super junction structure) of the n-type pillar layer **3** and the p-type pillar layer **4** has, for example, a striped configuration, but is not limited thereto, and may be formed in a lattice configuration or a staggered configuration.

[0026] A base layer **5** made of p-type silicon is provided on the p-type pillar layer **4** as a fourth semiconductor layer. A source layer **7** made of n^+-type silicon as a fifth semiconductor layer and a contact layer **6** made of p^+-silicon are selectively provided on a surface portion of the base layer **5**.

[0027] A trench is formed on a junction interface between the n-type pillar layer **3** and the p-type pillar layer **5**, and a control electrode (gate electrode) **9** is provided therein via a gate insulating film **8**. That is, a MOS gate section of this embodiment has a trench gate structure. Of a side wall of the trench, the side wall on a p-type pillar layer **4** side from the junction interface between the n-type pillar layer **3** and the p-type pillar layer **4** is in contact with the source layer **7**, the base layer **5** and the p-type pillar layer **4**, and the side wall on a n-type pillar layer **3** side from the junction interface between the n-type pillar layer **3** and the p-type pillar layer **4** is in contact with the n-type pillar layer **3**.

[0028] The control electrode **9** is, for example, formed by a planar pattern with a striped configuration like the n-type pillar layer **3** and the p-type pillar layer **4**, and provided above the junction interface between the n-type pillar layer **3** and the p-type pillar layer **4**. A bottom of the control electrode **9** is opposed to the junction interface between the n-type pillar layer **3** and the p-type pillar layer **4** via the gate insulating film **8**. Of a side face portion of the control electrode **9**, the side face portion on the p-type pillar layer **4** side from the junction interface between the n-type pillar layer **3** and the p-type pillar layer **4** is opposed to the source layer **7**, the base layer **5** and the p-pillar layer **4** via the gate insulating film **8**, and the side face portion on the n-type pillar layer **3** from the junction interface between the n-type pillar layer **3** and the p-type pillar layer **4** is opposed to the n-type pillar layer **3** via the gate insulating film **8**.

[0029] The first main electrode **1** is provided on an opposite face of the major surface of the drain layer **2**. The first main electrode **1** is in ohmic contact with the drain layer **2**, functions as a drain electrode in the MOSFET, and functions as a cathode electrode in the Schottky barrier diode.

[0030] The second main electrode **10** is provided on surfaces of the contact layer **6**, the source layer **7** and the n-type pillar layer **3**. The second main electrode **10** is insulated from the control electrode **9** by an interlayer insulating film provided on the trench.

[0031] The second main electrode **10** is in ohmic contact with the source layer **7** and the contact layer **6**, and functions as a source electrode in the MOSFET. The second main electrode **10** located between adjacent control electrodes **9** sandwiching the n-type pillar layer **3** is in contact with the surface of the n-type pillar layer **3** to form a Schottky junction **11** and function as an anode electrode of the Schottky barrier diode.

[0032] More specifically, the semiconductor device according to this embodiment has a structure where the MOSFET having a trench gate structure and a super junction structure and the Schottky barrier diode are integrated on one chip, and the MOSFET and the Schottky barrier diode are connected in parallel between the first main electrode **1** and the second main electrode **10**.

[0033] When prescribed control voltage is applied to the control electrode **9** in a state where electrical potential of the second main electrode **10** is set to be lower than that of the first main electrode **1**, a channel (inversion layer) is formed in a portion facing the control electrode **9** of the base layer **5** and the p-type pillar layer **4**, and electrons in the ON state of the MOSFET flow from the second main electrode **10** through the source layer **7**, the channel, the n-type pillar layer **3** and the drain layer **2** to the first main electrode **1**. The above control voltage is enough high for forming the channel (inversion layer) in the base layer **5**, the p-type pillar layer **4** has a lower p-type impurity concentration than the base layer **5**. Hence, it is possible to form the channel (inversion layer) also in the p-type pillar layer **4** by the above control voltage.

[0034] When the MOSFET is OFF, the Schottky barrier diode operates in a state where electrical potential of the second main electrode **10** is set to be higher than that of the first main electrode **1**, and a forward electron current flows from the second main electrode **10** through the n-type pillar layer **3** and the drain layer **2** toward the first main electrode **1**.

[0035] Further, in the super junction structure in the OFF state of the MOSFET, a depletion layer extends from the p-n junction of the n-type pillar layers **3** and the p-type pillar layer **4** in a state where electrical potential of the first main electrode **1** is set to be higher than the second main electrode and the high breakdown voltage can be held.

[0036] Here, as a comparative example, forming the base layer **5** and the source layer **7** on the n-type pillar layer **3** makes it impossible to form the Schottky junction **11**. Alternatively, when all of the base layer **5**, the source layer **7** and the Schottky junction **11** are formed on the surface of the n-type pillar layer **3**, the surface region is separated into the region operating as the MOSFET and the region operating as the Schottky barrier diode, and the MOSFET and the Schottky barrier diode cannot share the drift layer, causing reduction of each effective area and increase of the ON resistance.

[0037] On the contrary, in this embodiment, the base layer **5** and the source layer **7** are formed on the p-type pillar layer **4**, and the Schottky junction **11** is formed on the surface of the n-type pillar layer **3** sandwiching the trench gate therebetween. Thus, in a state where the ohmic contact for operating as the MOSFET and the Schottky junction for operating as the